

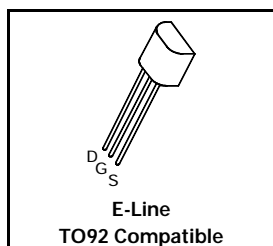
# N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

## ZVN4210A

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### FEATURES

- \* 100 Volt  $V_{DS}$
- \*  $R_{DS(on)} = 1.5\Omega$
- \* Spice model available



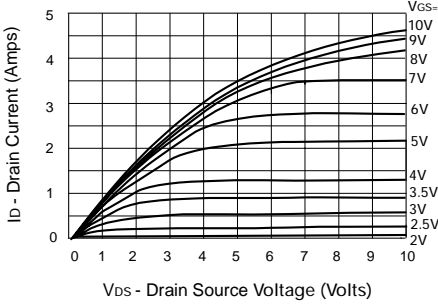
### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	100	V
Continuous Drain Current at $T_{amb}=25^{\circ}\text{C}$	$I_D$	450	mA
Pulsed Drain Current	$I_{DM}$	6	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}\text{C}$	$P_{tot}$	700	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}\text{C}$

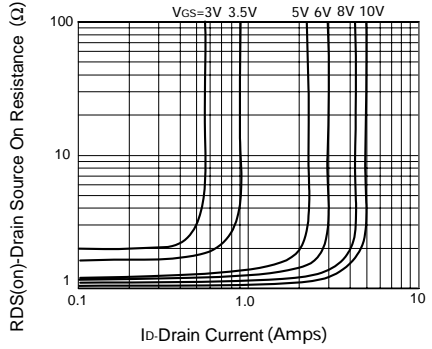
### ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	100		V	$I_D=1\text{mA}, V_{GS}=0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.8	2.4	V	$I_D=1\text{mA}, V_{DS}=V_{GS}$
Gate-Body Leakage	$I_{GSS}$		100	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$		10 100	$\mu\text{A}$ $\mu\text{A}$	$V_{DS}=100\text{V}, V_{GS}=0$ $V_{DS}=80\text{V}, V_{GS}=0\text{V}, T=125^{\circ}\text{C}(2)$
On-State Drain Current(1)	$I_{D(on)}$	2.5		A	$V_{DS}=25\text{V}, V_{GS}=10\text{V}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		1.5 1.8	$\Omega$	$V_{GS}=10\text{V}, I_D=1.5\text{A}$ $V_{GS}=5\text{V}, I_D=500\text{mA}$
Forward Transconductance(1)(2)	$g_{fs}$	250		mS	$V_{DS}=25\text{V}, I_D=1.5\text{A}$
Input Capacitance (2)	$C_{iss}$		100	pF	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$
Common Source Output Capacitance (2)	$C_{oss}$		40	pF	
Reverse Transfer Capacitance (2)	$C_{rss}$		12	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		4	ns	$V_{DD}\approx 25\text{V}, I_D=1.5\text{A}$
Rise Time (2)(3)	$t_r$		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		20	ns	
Fall Time (2)(3)	$t_f$		30	ns	

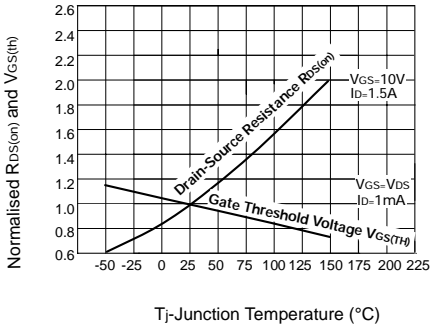
## TYPICAL CHARACTERISTICS



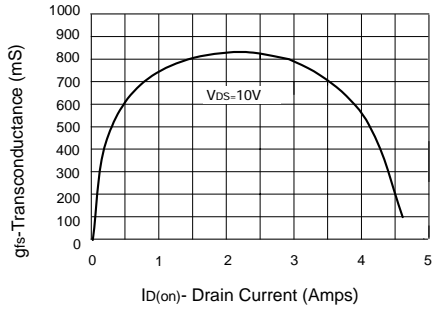
**Saturation Characteristics**



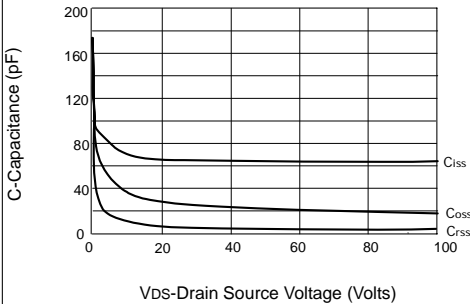
**On-resistance v drain current**



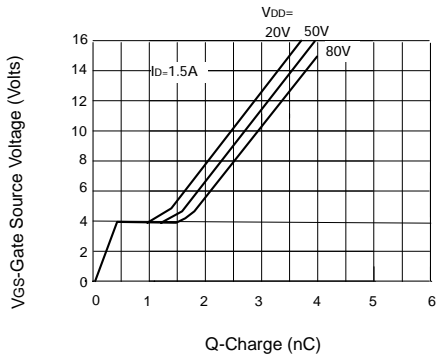
**Normalised  $R_{DS(on)}$  and  $V_{GS(th)}$  v Temperature**



**Transconductance v drain current**



**Capacitance v drain-source voltage**



**Gate charge v gate-source voltage**